Silicon Photonics
Opportunity, Applications & Recent Results

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Agenda

- Opportunity for Silicon Photonics
- Copper vs optical
- Recent advances
- Intels SP Research
- Recent results
  - Intel’s Silicon Laser
- Summary
**ELECTRONICS: Moore’s Law Scaling**

Integration & increased functionality

Volume economics – faster, better, cheaper

-MIPS

$/MIPS

Intel® 386™ DX Microprocessor

Intel® 486™ DX CPU

Pentium® Processor

Pentium® II Processor

Pentium® III Processor

Pentium® Pro Processor

Pentium® 4 Processor

Intel® 386™ DX Microprocessor

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The Opportunity of Silicon Photonics

- Take advantage of enormous ($ billions) CMOS infrastructure, process learning, and capacity
  - Available tools: litho requirements typically >90nm
  - Draft continued investment going forward
- Potential to integrate multiple optical devices
- Micromachining could provide smart packaging
- Potential to converge computing & communications

Industry standard silicon manufacturing processes could enable integration, bring “volume economics” to optical.

To benefit from existing infrastructure optical wafers must run alongside product.. i.e CMOS fabrication compatible..
Today's High Speed Interconnects

Decreasing Distances →

Need to drive volume economics to drive optical closer to chip
Copper Approaching Limits

Simulation of 20” channel transmitter w/ equalization

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<th>Standard FR4</th>
<th>FR4</th>
<th>Low Loss Ro4350</th>
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Channel Attenuation [dB]

Red Zone = Eye Closes

Copper scaling more challenging. Headroom getting squeezed.

Howard Heck
**Electrical to Optical**

- **Enterprise**
  - Distance: 0.1-10km
  - 10G >= 40G
  - Silicon Photonics?

- **Rack-Rack**
  - Distance: 1-100m
  - 3.125G 10G 40G
  - Optical Tech

- **Board-Board**
  - Distance: 50-100cm
  - 3.125G 5-6G 10G 20G
  - Transition Zone

- **Chip-Chip**
  - Distance: 1-50cm
  - 3.125G 5-6G 10G 15-20G
  - Copper Tech

**Transition driven by cost**

- 2005
- 2010+

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The Photonic Dilemma

- Fiber has much more bandwidth than copper

- However, it is much more expensive....
**Photonics:** The technology of emission, transmission, control and detection of light (photons) aka fiber-optics & opto-electronics

**Today:** Most photonic devices made with exotic materials, expensive processing, complex packaging

**Silicon Photonics Vision:** Research effort to develop photonic devices using silicon as base material and do this using standard, high volume silicon manufacturing techniques in existing fabs

**Benefit:** Bring volume economics to optical communications
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Silicon Pro’s and Cons

+ Transparent in 1.3-1.6 μm region
+ CMOS fabrication compatibility
+ Low cost
+ High-index contrast – small footprint

- No electro-optic effect
- No detection in 1.3-1.6 μm region
- High index contrast – coupling
- Lacks efficient light emission

Silicon will not win with passive devices..
Must produce active devices that add functionality
Silicon Photonics Breakthroughs Are Accelerating

Progress In Recent Years Is Accelerating still not there...
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Intel’s Silicon Photonics Research

1. Develop photonic building blocks in silicon

1) Light Source
2) Guide Light
3) Modulation
4) Photo-detection
5) Low Cost Assembly
6) Intelligence

1GHz (Nature ’04)
4 Gb/s (’05)

First Prove that silicon is viable material for photonics

First Continuous Silicon Laser
(Nature 2/17/05)

SiGe Photodetectors

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In addition to device costs, packaging and testing costs must drop with to enable high volume photonics.
Micromachining for Packaging

Use standard pick and place technologies along with litho defined silicon micro-machining

- U-Grooves
- V-Grooves
- 45° Mirrors
- Facet Preparation
- Tapers
- Laser Attach
Intel’s Silicon Photonics Research

1. Develop photonic building blocks in silicon

2. Integrate increasing functionality directly onto silicon
Intel’s Silicon Photonics Research

1. Develop photonic building blocks in silicon
2. Integrate increasing functionality directly onto silicon
3. Long term explore monolithic integration
SILICON LASER
What we announced on Feb 17th
The First Laser


this ruby laser used a flash lamp as an optical pump

Fully Reflective Mirror

Partially Reflective Mirror

Flash Lamp

RUBY CRYSTAL ROD

LASER BEAM
Raman: (Historical Note)

Raman Effect or Raman Scattering: A phenomenon observed in the scattering of light as it passes through a transparent medium; the light undergoes a change in frequency and random alteration in phase due to a change in rotational or vibrational energy of the scattering molecules.

• Discovered a material effect that is named after him
  • *Nature* published his paper on the effect on March 31, 1928
  • He received the Nobel prize in 1930 for his discovery
• The first laser using the Raman effect was built in 1962
• Today Raman based amplifiers are used throughout telecom
  • Most long distance phone calls will go through a Raman amplifier
**The Raman Effect**

**Materials**

- Silicon
- Indium Antimonide (III-V)
- Quartz
- Lithium Niobate (used for modulators)
- Diamond
- Glass Fiber (Raman lasers/amps)

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The Raman effect is 10,000 times stronger in silicon than in glass fiber. This allows for significant gain in centimeters instead of kilometers.

Fabrication of low-loss silicon waveguides is challenging.

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Raman Gain in Silicon

(b) Raman Gain and WG loss vs. Input Pump Power

CW Gain Saturation due to TPA induced FCA
Two Photon Absorption

In silicon, one infrared photon doesn’t have the energy to free an electron. But, occasionally, two photons can knock an electron out of orbit.

Free electrons absorb individual photons and cancel Raman gain.
Overcoming TPA induced FCA

Pump power

Raman Gain

Gain needed to make a laser

Gain limit due to Two Photon Absorption problem

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Effective Carrier lifetime reduction

PIN Cross-section

TPA coeff ~ 0.5 cm/GW, α 0.39 dB/cm, FCA cross sect 1.45e-17 cm^2 @ 1550 nm. The lifetime is used as a fitting parameter.

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CW gain vs. reverse bias voltage
WG= ~1.5um by 1.5um

Pump λ=1550 nm  Signal λ=1686 nm

Pump λ=1550 nm  Signal λ=1686 nm
With gain can build Laser:
Silicon Waveguide Cavity

With gain can build Laser:
Silicon Waveguide Cavity

24%/71%
90%

Dichroic coating
p-region

Broad-band reflective coating

Pump beam
Laser output

16 mm

V bias
n-region

R_f
R_b
Experimental setup

- Pump at 1,550 nm
- High reflection coating
- Silicon waveguide
- Laser output at 1,686 nm
- Dichroic coating
- High reflection coating
- Laser output power meter
- Tap coupler
- Polarization controller
- De-multiplexer
- LP filter
- Optical spectrum analyzer
- Pump power monitor
Experimental Set up

Test chip with 8 laser WG’s

Laser chip
Typical Lasing Criteria

• Threshold behavior:
  ➢ rapid growth in output power when gain > loss

• Spectral linewidth narrowing:
  ➢ Coherent light emission
Threshold, Efficiency, and PIN effect

Laser turns on at threshold, when gain per pass in cavity becomes greater than the loss.
Spontaneous emission vs. laser spectrum

When lasing, the spectrum becomes much more narrow and much higher in power.
Wavelength tuning (comparison)

Silicon Raman laser

Commercial ECDL

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Potential Applications
Communications Applications

Si Raman Amplifier

Si Multi-Channel Transmitter

Si Raman Modulator

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Covering the Gaps

• Different wavelengths require different types of lasers
• Mid-Infrared very difficult for compact semiconductors
• Raman Lasers could enable lasers at these wavelengths
• Applications in sensing, analysis, medicine, and others

Compact Semi. Lasers

Could enable lasers for a variety of applications
Summary

Long term true convergence opportunities are with silicon
B/W will continue drive conversion of optical into interconnects
Tremendous progress from research community
  ➢ Need to continue pushing & improving performance
Research breakthrough with CW silicon laser
Integration is next set of challenges
In order to benefit Technologies must be CMOS fabrication compatible to benefit from HVM & infrastructure

Silicon will not win with individual devices, but with integrated modules that bring increased total functionality & intelligence at a lower cost
**Benefits of Integration**

- **Photonic Integration:**
  - Reduction in interfaces – lower loss
  - Reduction in size
  - Simpler assembly, testing, packaging
  - Cost

- **Optoelectronic Integration:**
  - Reduce parasitics, improved high-freq performance
  - Further size, testing, packaging reductions
  - Cost

Integration is only useful if integrated device has benefit (functionality, cost, performance) over discrete devices.
CMOS Integration Challenges

- Film topology
- Coupling to fiber
- Contaminating the fab
- Yield metrology
- Thermal budgets
- Heat dissipation
- Complexity / yield

Optoelectronic Integration

To benefit from existing infrastructure optical wafers must run alongside product, introducing additional pragmatic challenges
Surface Topology: Litho vs DOF

- Depth of focus (DOF) shrinks as litho improves
- Many optical devices are much taller than transistors

For 0.18µm and better, topology exceeds DOF
New planarization techniques required for advanced litho
Fiber Coupling

Getting light from fibers into silicon waveguides will require couplers. For certain structures litho and etch parameters must be carefully controlled.

- Coupling from standard fiber to Si waveguides requires special structures (tapers, gratings, etc).
- For wedge tapers, etch angle as well as the tip lithography impact loss.
- Sidewall roughness is also a factor.

Taper from (W x H):
10 x 8 μm to 2.5 x 2.3 μm
Assume zero roughness

Source: Intel
Yield Metrology

- CMOS fabs monitor thousands of parameters across wafer in line
- Tight control – e.g. CMOS gate width held to 10’s of angstroms
- Significant per-wafer cost savings from screening out yield early

- In-line wafer level optical probing is very immature
- Most optical device testing is performed after wafer dicing

To truly gain from HVM processing, automated & non-destructive techniques for probing optical devices at the wafer level must be developed
Opto-Electronic Integration (cont)

**Thermal:**
For optoelectronic integration, optical devices must tolerate heat generated by CMOS circuits.

**Process compatibility:**
@ 10Gb/s CMOS IC’s need 90nm technology
Silicon Photonic devices may only need ~.25um

**Yield:**
Typical industry IC yields are high, but the process windows are extremely tight.
Tweaks to enable opto-electronic integration may effect IC yield

Trade off of yield and process complexity will determine if opto-electrical integration valuable
Animation

Click in box while in slide show mode to start

Click outside animation box after animation
Extending and Expanding Moore’s Law

Discrete  SSI  LSI  VLSI

Sensors  Mechanical  Biological  Fluidics  Wireless  Optical

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Two Photon Absorption in Silicon

Two photons can simultaneously hit an atom
Combined energy enough to kick free an electron

Pump
\( \lambda = 1.55 \mu \text{m} \)

Silicon band gap
1.1 eV

Conduction band

Valence band